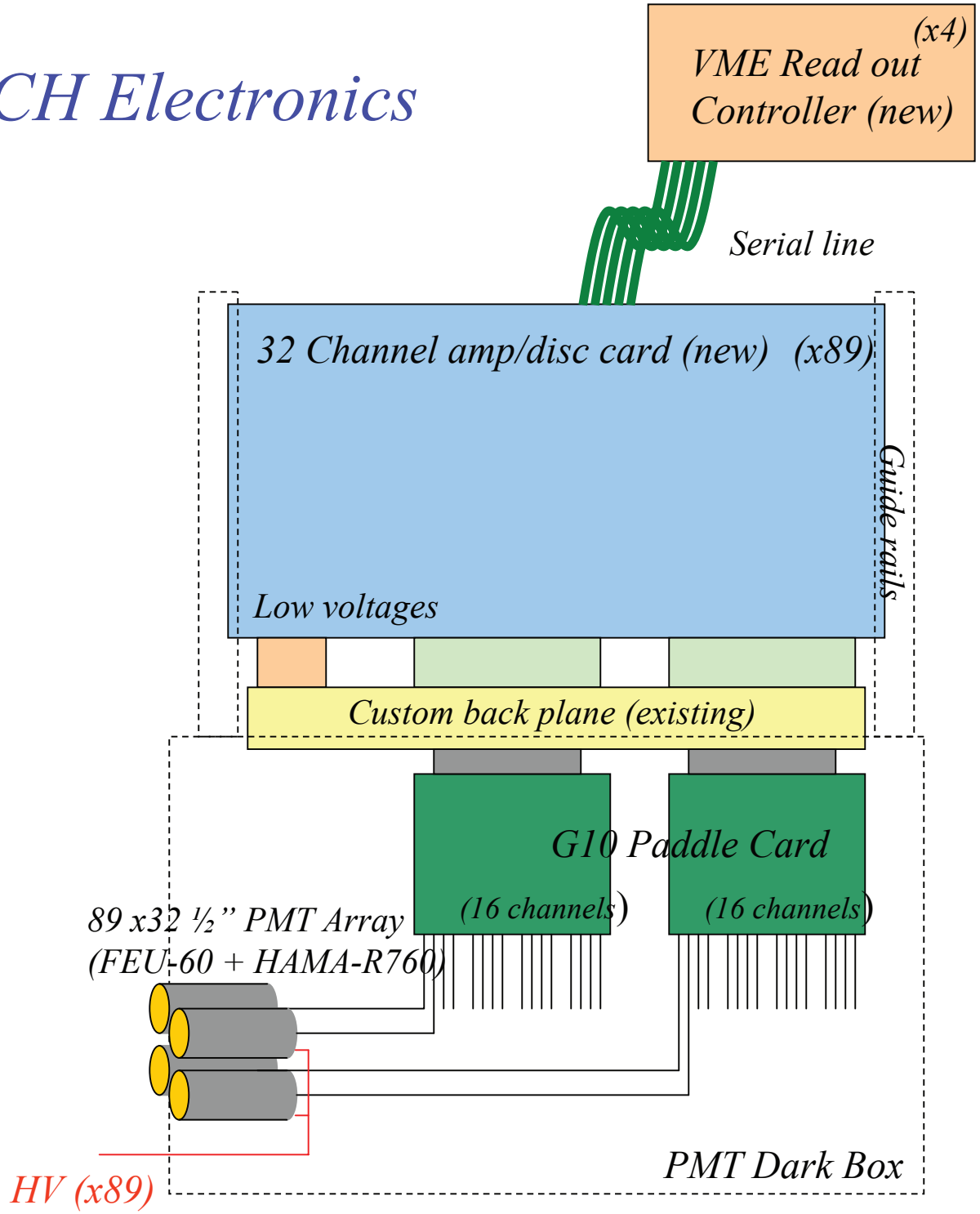
RICH Update

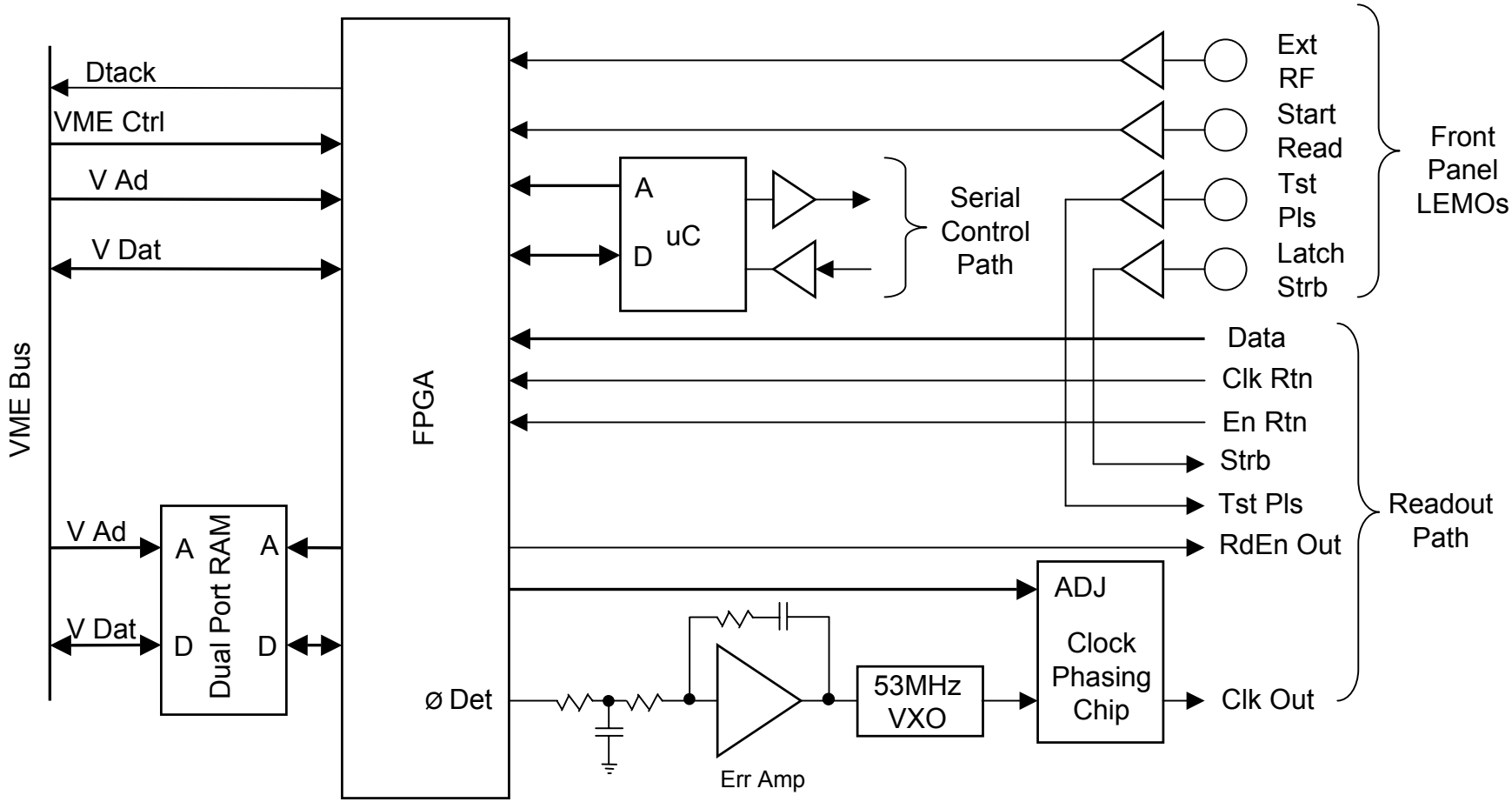
Mark Messier (for Sten Hansen, Andre Lebedev, and Sharon Seun)
MIPP Collaboration Meeting
10 August 2002
FNAL

- Electronics Status
- HV
- Monte Carlo

Layout of RICH Electronics



907 RICH Readout Card Block Diagram



E907 RICH Electronics Status

Parts for prototypes are here

Layout for 32 channel card finished

I need to check the layout. We can presumably get PC fab quotes this coming week, and have Harvard bankroll the order as with the readout cards.

5 Readout cards are here and 1 is assembled

Engineering co-op is writing equations for readout card fpga
(another week probably)

Terry Kiper has not yet started on uC code for readout card or 32 chan cards, but he can begin soon (this week perhaps)
The programming effort is 2-3 weeks of work including both cards

If we do things correctly, we will finish the readout card firmware about the time the 32 channel cards arrive.

S. Hansen 07-08-02

A list of ongoing tasks that relate to the E907 RICH boards:

32 channel card:
Prototype design, schematic drawing and PC layout is complete. Parts for the prototypes are on hand.

Assembly of 2 prototype cards : 1 week in Bob Jones' tech shop.
Bench testing/debugging of prototypes: 1 week.
In situ testing on RICH: 3 days.
Preparation of parts orders for production quantities: 2 days

Assume contract for board fab, assembly and testing is done by Harvard.

Readout card:

5 prototype cards are here, 1 is 90% assembled (we are missing a couple of LVDS chips).

Logic chip equations: 40% complete, another week to complete.

If the present iteration of the board works with few modifications, we can assemble the rest here, or ship the parts and blank boards to Harvard. This is a relatively small job.
If there are an unacceptable number of modifications required for proper operation, we will have to iterate on the PCB fab, presumably in the same manner as before.

Preparation of parts orders for 5 boards: ½ day. (we scrounged parts for the 1 that is assembled).

Effort required for both boards:

Microcontroller code: 0% complete. Terry Kiper is the person for this work. I would estimate 2-3 weeks of his time to adapt code that we have on other boards these specific boards. He can probably get started sometime next week.

08/07/2002.
Sten Hansen,

A VME memory map of the controller DP RAM

(Hex arithmetic has not been carefully checked)

1. Data Area (grows upward)

0x0: Bits 0..10: Leading word count (word count is tentatively inclusive of itself)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used					WdCnt10..WdCnt0										

0x2..0xN: Header Block;

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD															

.
.

0xN+2: Data Block;

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Board ID						Hit Address									

.
.

0xN+0x800: End of largest possible Data Block (hit on all channels);

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Board ID						Hit Address									

2. Control and Status Area (grows downward)

0x7FFE: Microcontroller Command Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD												Command code			

Command code list so far:
0x0: Initialize amp/disc cards
(determine # of responding boards, assign logical addresses to boards)
0x1: Write thresh block
0x2: Read thresh block
0x3: Write thresh single channel
0x4: Read thresh single channel
0x5: Write enable bits block
0x6: Read enable bits block
0x7: Write channel enable bits single card
0x8: Read channel enable bits single card
0x9: Write pipeline delays block
0xA: Read pipeline delays block
0xB Write pipeline delay single card
0xC Read pipeline delay single card

0x7FFC: Microcontroller status (read only from VME)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD													Busy	Command Accepted	Command Completed

0x7FFA: Microcontroller Board Count (read only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used											# of Responding Boards				

0x7FF8: Microcontroller Address Specifier (significant only during single operations)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	DP Ram Address													

0x7FF6: Board ID (This value is appended to the channel address)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used										Board ID					

TBD:

Some number of words containing the constant part of the header block

Addresses that follow will need adjustment by the number of words used by header information.

0x7FF4: Pipeline delay values (board 0x0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used								Pipeline delay setting							

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.

0x7FB4: Pipeline delay values (board 0x1F)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used								Pipeline delay setting							

0x7FB2: Enable bits (board 0x0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel Enable Bits for inputs 15..0															

0x7FB0: Enable bits (board 0x0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel Enable Bits for inputs 31..16															

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0x7F32: Enable bits (board 0x1F)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel Enable Bits for inputs 15..0															

0x7F30: Enable bits (board 0x1F)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel Enable Bits for inputs 31..16															

0x7F2E: Thresholds (board 0x0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Threshold for Chan 1								Threshold for Chan 0							

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0x7F0E: Thresholds (board 0x0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Threshold for Chan 31								Threshold for Chan 30							

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0x7B2E: Thresholds (board 0x1F)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Threshold for Chan 1								Threshold for Chan 0							

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0x7B0E: Thresholds (board 0x1F)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Threshold for Chan 31								Threshold for Chan 30							

The following values are updated periodically by the uC (of order 1Hz)

0x7B0C: Power supply readback (board 0x0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-5 Supply Value (40 mV/Count)								+5 Supply Value (40mV/Count)							

.

.

0x7AEC: Power supply readback (board 0x1F)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-5 Supply Value (40 mV/Count)								+5 Supply Value (40mV/Count)							

0x7AEA: Ambient temperature ADC readback (board 0x0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				°C = (ADC Counts – 1615) · 0.1719											

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0x7ACA: Ambient temperature ADC readback (board 0x1F)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				°C = (ADC Counts – 1615) · 0.1719											

Notes:

The starting address for each data type in the control section of the RAM area is fixed. The significant length of each block is dependent on the number of active cards in the control chain.

Front End Board Testing

- Power PC loaned to Harvard by LNL in May

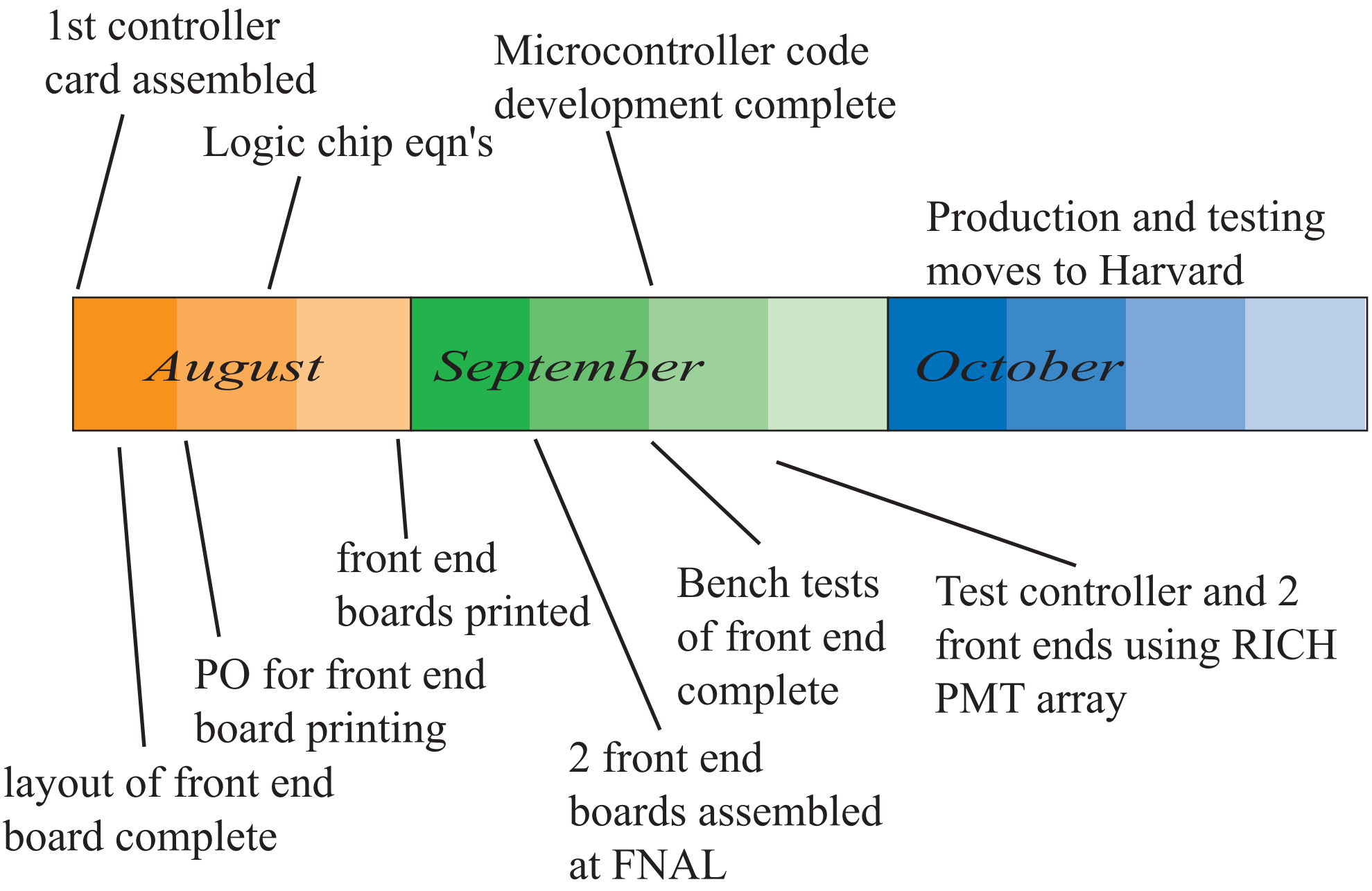
- Andre L. has kernal and file system built and working

- Waiting for controller card to play with

- Andre (and Sharon?) will write testing code

- This code will be re-used in the DAQ for the RICH

Plan For RICH Electronics



RICH HV

- HV supplies in SELEX portacamp. 7 of 8 power up

- located SELEX HV manual

- Interupt system works and I think I understand it

- Andre has looked into a few other options:

Power Supply	HV (kV)	Current (mA)	Price($)
Bertan			
102-02	2	500	4,000 x 6
102-03	3	333	4,000 x 6
Glassman			
PS/EW02R300-115	2	300	2,300 x 6
PS/EK02R300-115	2	300	2,300 x 6
CAEN	2.5	13/chan	45,600
Matsuada			
AU-3	3	200	3,100 x 6
AU-2	2	300	3,100 x 6
W	350 Watts		1,000 x 6

RICH MC Work

Sharon S. has imported code from SELEX for RICH hits as well as digitization code to MIPP Monte Carlo

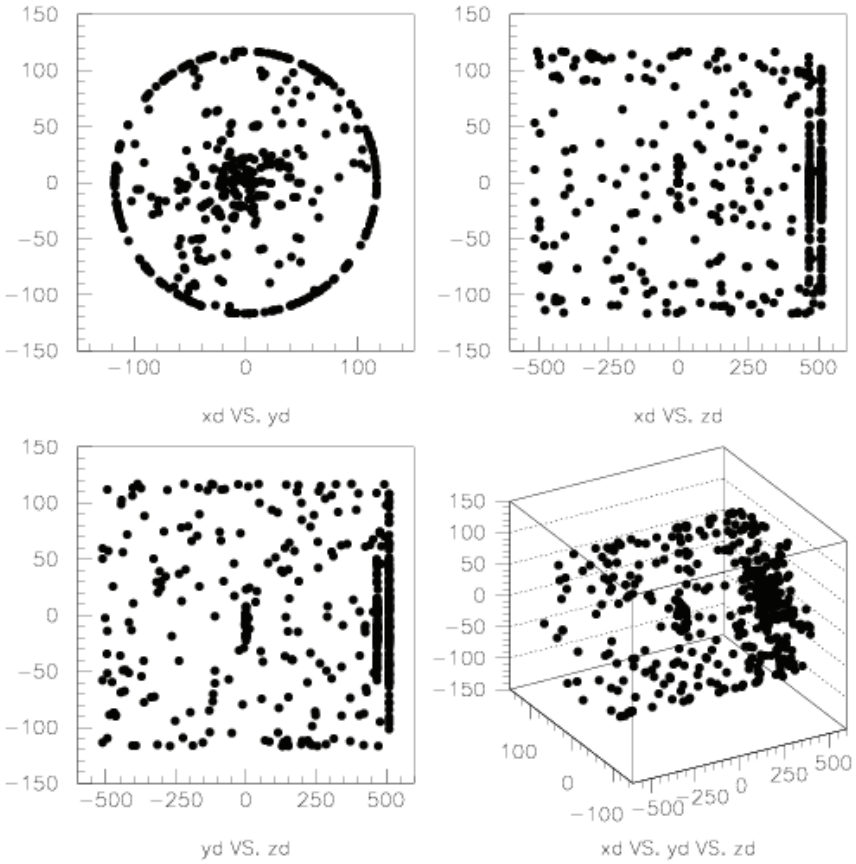
All compiles, links, and runs, but...

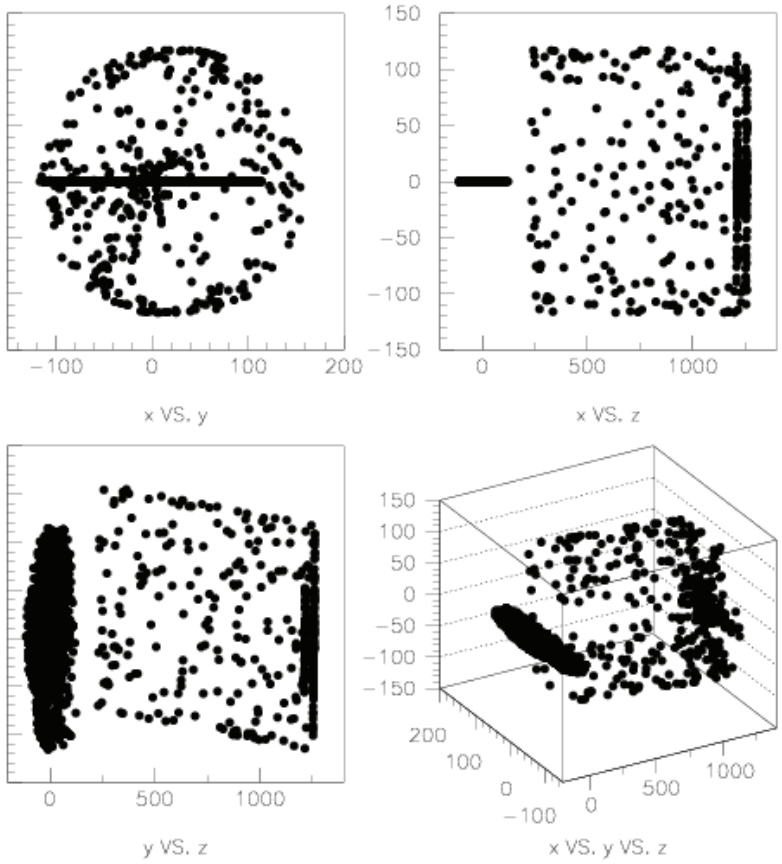
Results don't look right. Most likely a bug in the hit packing.

Sharon takes her oral qualifying exam next week and will get back to working on the code. Hope to make study of CO2 by middle of September

Sharon also has SELEX reconstruction code in hand and has begun to understand how it works. Probably easiest to rewrite this once the algorithms are understood. Might be easier just to check π/K/p hypotheses rather than fit ring radii.

RICH Hits





Hits in daugher frame

Hits in mother frame

To me, looks like error in hit packing...

(Sharon Seun)

Calling sequence for SELEX reconstruction code